

Joint Inventors

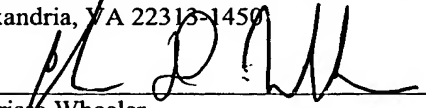
Docket No. 20063/10013

"EXPRESS MAIL" mailing label No.

EV 403727884 US

Date of Deposit: December 29, 2003

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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that We, **Hyuk PARK**, a citizen of the Republic of Korea, residing at #301 759-12 Bono-dong, Sangnok-gu, Ansan-si, Gyeonggi-do 426-180, Korea; and **Bong Kil KIM**, a citizen of the Republic of Korea, residing at 332 Choi-dong, Hanam-si, Gyeonggi-do 465-220, Korea, have invented new and useful **MEMORY CELL STRUCTURES INCLUDING A GAP FILLING LAYER AND METHODS OF FABRICATING THE SAME**, of which the following is a specification.

MEMORY CELL STRUCTURES INCLUDING A GAP FILLING LAYER AND METHODS OF FABRICATING THE SAME

FIELD OF THE DISCLOSURE

[0001] This disclosure relates to a method of fabricating an embedded flash memory and, more particularly, to a method of fabricating a flash memory cell, which can effectively prevent the formation of voids in a gap between spacers for a gate constituting a transistor of a flash memory cell.

BACKGROUND

[0002] Non-volatile memory devices such as EEPROMs or flash EEPROMs comprise memory cells including a floating gate which stores data and a control gate which applies voltage to the floating gate. The memory cells are formed on a semiconductor substrate including source/drain regions.

[0003] Figs. 1a and 1b are cross-sectional views of a prior art flash memory cell during fabrication.

[0004] Referring to Fig. 1a, an N-well 12 and a P-well 13 are formed in a silicon substrate 11. The N-well 12 and/or the P-well 13 may be formed, for example, by ion implantation. A source/drain region 14 is defined in the P-well 13 by, for example, ion implantation. A gate oxide 15, a floating gate 17, an oxide-nitride-oxide (ONO) layer 18, and a control gate 19 are then formed by ion implantation, photoresist coating, patterning, development, deposition, etc. The floating gate 17 stores electric charges and the control gate 19 is used to apply voltage to the floating gate 17. The floating gate 17

and the control gate 19 are formed into a tandem structure. Spacers 20 of SiN are formed to isolate and protect the gate area including the floating gate 17 and the control gate 19. A source/drain region 14 is defined in the upper part of the P-well 13, and positioned between adjacent gate spacers 20 of adjacent gate areas. A unit block of a transistor consists of the floating gate 17, the control gate 19, and the source/drain region 14. In addition, silicide 16 and a borderless contact (BLC) layer 21 are formed to connect the flash memory cell to an external terminal such as a word line or a bit line.

[0005] Referring to Fig. 1b, after the formation of the spacers 20, borophosphorsilicate glass (BPSG) 22 is deposited over the substrate. Generally, in order to ensure the characteristics of the logic transistors and to reduce the costs in fabricating an embedded flash memory, a SiN layer is deposited and etched to form the spacers 20. The BPSG layer 22 is then deposited over the gate structure to form a passivation layer of the flash memory cell.

[0006] However, because the gap between the SiN spacers is very narrow in a cell array, if the BPSG layer 22 is deposited after formation of the spacers 20, voids 23 are formed in the gap between the SiN spacers 20. The voids 23 may change the characteristics of each cell. In addition, the size of the voids 23 vary according to a critical dimension of polysilicon constituting each cell. This variation in the sizes of the voids may also change characteristics of the cells. For example, the voids function as parasitic capacitances which decrease the operating speed of the flash memory device

and function as points of stress and leakage during device operation, thereby causing deterioration of device reliability and characteristics.

[0007] To obviate the problems due to voids formed in the passivation layer in fabricating a non-volatile memory device, Mei et al., U.S. Patent 6,475,895, describes a semiconductor device having a passivation layer and a method for its fabrication. This U.S. patent provides a final passivation layer, especially for flash memory and other non-volatile memory technologies, that can overcome problems due to a narrow gap between metal lines which cannot be completely filled by using the conventional film deposition techniques of chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD). A semiconductor device structure described in the above-mentioned U.S. patent includes a first layer of high density plasma (HDP) oxide and an overlying layer of silicon oxynitride. Application of the HDP oxide to a pattern of metal structures fills gaps between the metal structures and allows for the void free deposition of the silicon oxynitride layer. The silicon oxynitride layer provides a hard outer coating to the passivation coating.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figs. 1a and 1b are cross-sectional views of a prior art flash memory structure during the fabrication process.

[0009] Figs. 2a through 2d are cross-sectional views of an example flash memory during an example fabrication process in accordance with the teachings of the present disclosure.

DETAILED DESCRIPTION

[0010] Referring to Fig. 2a, an N-well 12 and a P-well 13 are formed in a silicon substrate 11. The wells 12, 13 may be formed, for example, by ion implantation. A source/drain region 14 is defined in the silicon substrate 11, for example, by ion implantation. Then, a gate oxide 15, a floating gate 17 which stores electric charges, an ONO layer 18, and a control gate 19 to apply voltage to the floating gate 17 are sequentially formed on the substrate 11 through photoresist coating, mask patterning, development, and deposition processes. Silicide 16 including a conductive metal element and a BLC layer 21 are then formed. The silicide 16 and the BLC layer 21 may be connected to an external terminal such as a word line or a bit line. Next, a SiN layer is deposited and etched to form spacers 20 in order to isolate and protect the gate areas (a gate area includes, for example, a floating gate 17 and a control gate 19).

[0011] Referring to Fig. 2b, a filling layer 24 is deposited over the gate areas and the spacers 20. Undoped polysilicon or amorphous silicon is used to form the filling layer 24. Narrow gaps between the spacers 20 can be easily filled up without voids being created because both undoped polysilicon and amorphous silicon have an excellent gap filling characteristics.

[0012] Referring to Fig. 2c, the filling layer 24 is etched. The etching of the sidewalls of the spacers 20 is restricted because of a high etching selectivity of the undoped polysilicon or the amorphous silicon with the SiN of the spacers 20. Therefore, if an anisotropic etching method with good selectivity is performed, the undoped polysilicon or the amorphous silicon,

which fills the gaps between the spacers 20, remains without being removed by the etching process. The etching solution used to etch the undoped polysilicon or the amorphous silicon is preferably $\text{HNO}_3 + \text{CH}_3\text{COOH} + \text{HF}$.

[0013] Referring to Fig. 2d, a BPSG layer 22 is deposited over the BLC layer 21, the upper silicide 16 on the gate areas, and the etched filling layer 24. Consequently, as shown in Fig. 2d, the gaps between the gate areas are completely filled with the filling layer 24 without any voids.

[0014] After formation of the BPSG layer 22, metal contact lines are formed in order to connect the flash memory cell to external terminals. The contacts between the metal contact lines on the silicide 16 are established for connection.

[0015] As described in the above, the illustrated method can effectively prevent the formation of voids in the gaps between gate spacers of adjacent gate areas during the deposition of a BPSG layer in fabricating an embedded flash memory cell. Accordingly, the illustrated method can obviate the effects of voids on cell characteristics and ensure stable operation of the memory device.

[0016] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed method prevent changes of cell characteristics due to voids by obviating the formation of voids in gaps between gate spacers in the deposition of BPSG. In particular, the illustrated method of fabricating a flash memory cell comprises: forming spacers to isolate and protect a gate area; depositing undoped polysilicon; etching the polysilicon by an anisotropic etching; and depositing BPSG.

[0017] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.